Nonlinear Design Technique for High-Power Switching-Mode Oscillators

Sanggeun Jeon, *Member, IEEE*, Almudena Suárez, *Senior Member, IEEE*, and David B. Rutledge, *Fellow, IEEE*

***Abstract*—A simple nonlinear technique for the design of high-efficiency and high-power switching-mode oscillators is presented. It combines existing quasi-nonlinear methods and the use of an auxiliary generator (AG) in harmonic balance. The AG enables the oscillator optimization to achieve high output power and dc-to-RF conversion efficiency without affecting the oscillation frequency. It also imposes a sufficient drive on the transistor to enable the switching-mode operation with high efficiency. Using this AG, constant-power and constant-efficiency contour plots are traced in order to determine the optimum element values. The oscillation startup condition and the steady-state stability are analyzed with the pole-zero identification technique. The influence of the gate bias on the output power, efficiency, and stability is also investigated. A class-E oscillator is demonstrated using the proposed technique. The oscillator exhibits 75 W with 67% efficiency at 410 MHz.**

***Index Terms*—Class-E tuning, high-efficiency oscillator, nonlinear optimization, oscillation stability, startup criterion.**

I. Introduction

RF AND microwave high-power sources have diverse applications in the industrial and scientific fields, including induction heating, electric welding, RF lighting, and plasma generation [1], [2]. For power sources, the efficiency is an important aspect because high power loss and its resulting thermal stress will degrade the reliability of transistors and increase the cost for thermal management.

A number of papers [3]–[9] have been devoted to improve the dc-to-RF conversion efficiency of oscillators by adopting the switching-mode amplifier concepts. In [3] and [4], class-E oscillators are designed by synthesizing the required phase shift with a feedback network. However, the assumption of lumped elements and the approximate calculation of the transistor phase shift make the technique difficult to apply to high-frequency oscillators. In [5] and [6], an experimentally tunable feedback network is added to standalone class-E and class-F amplifiers, respectively, to give an oscillation at higher frequency. The small-signal circular function [5] and the required attenuation of the feedback network [6] are calculated to fulfill the oscillation condition, but no systematic nonlinear technique is proposed for the design. In [7], the design criterion is also linear and based on the calculation of a small-signal loop gain providing high efficiency in the high-power oscillator. On the other hand, [8] and [9] present systematic nonlinear-design procedures based on the load–pull optimization of the transistor harmonic terminations. These load–pull techniques are versatile and powerful since they are not constrained to a specific embedding topology. However, the performance of the final design is closely dependent on the synthesis accuracy at the different harmonic frequencies.

In this paper, a new systematic nonlinear technique to optimize the output power and efficiency of switching-mode oscillators is proposed. Although constrained to a specific feedback-network topology, the technique enables a simple and reliable design of high-efficiency oscillators, taking into account an arbitrary number of harmonic components. It combines existing quasi-nonlinear methods [10], [11] with the use of an auxiliary generator (AG) [12] in harmonic balance (HB). An AG is an ideal voltage generator introduced into the circuit only for simulation purposes. It operates at the oscillation frequency and fulfills a nonperturbation condition of the steady-state solution [12]. In the optimization of the switching-mode oscillators, the AG has a twofold role. First, the AG is used to set the oscillation frequency to the desired steady-state value. Hence, circuit parameters can be optimized to maximize the output power and efficiency without affecting the oscillation frequency. Second, the AG with large voltage amplitude drives the transistor in deep saturation region, which leads to the switching-mode operation with high efficiency.

To achieve a robust convergence of the HB system including the AG, the provision of suitable initial values is of importance. Accordingly, a quasi-nonlinear design is initially performed using the techniques developed in previous papers [10], [11]. This gives the proper circuit topology and the initial values for the circuit elements. Here, a nonlinear optimization of the amplifier is also carried out, tracing contour plots of the output power and drain efficiency versus critical circuit elements. The appropriate embedding network for the oscillator circuit is then determined from the resulting terminal voltages and currents.

The oscillator optimization is performed with an AG, the amplitude of which is made equal to that of the input-terminal voltage in the former amplifier design. This ensures the switching-mode operation of the transistor. Using the AG, the circuit parameters are tuned to achieve high output power and efficiency at the specified oscillation frequency. Contour plots are traced to determine the optimum element values. The oscillation startup and steady-state stability are verified with

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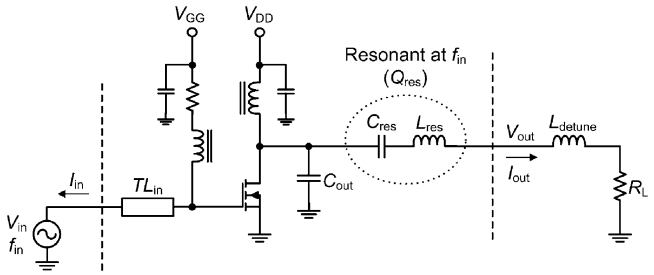

Fig. 1. Schematic of the class-E amplifier. The input-drive frequency is set to the oscillation frequency. $\mathrm{TL}_{\mathrm{in}}$ is a transmission line added at the gate to facilitate the layout of the feedback network, which will be synthesized in Section II-B. Dashed lines represent the reference planes for the synthesis.

the pole-zero identification technique [13], [14]. The influence of the gate bias on the oscillator output power, efficiency, and stability is analyzed, together with the causes for the common observation of hysteresis versus the gate bias in high-power oscillators. The techniques have been applied to the design of a class-E oscillator, which showed an output power of 75 W from a single transistor and 67% dc-to-RF conversion efficiency at 410 MHz.

This paper is organized as follows. Section II presents the optimization of the initial class-E amplifier and the synthesis of the embedding network. Section III presents the nonlinear optimization of the class-E oscillator, the verification of the oscillation startup, and the stability analysis of the steady-state solution. Section IV presents the analysis of the influence of the gate bias on the oscillator output power and efficiency. Finally, Section V presents the experimental results.

II. Optimization of Class-E Amplifier and Synthesis of Embedding Network

The class-E oscillator considered in this study consists of a transistor that operates in the saturation region, and an embedding network that includes the output load. The transistor in an oscillator operates in the same way as in an amplifier under the same set of terminal voltages and currents [10]. Thus, a class-E amplifier with optimized performance is first designed. The embedding network is then synthesized, applying the substitution theorem to the optimized terminal voltages and currents [11]. It should be noted that this synthesis considers only the fundamental frequency, thus the performance of the designed oscillator will be further investigated with the proposed fully nonlinear technique in Section III.

A. Optimization of Class-E Amplifier

The schematic of the class-E amplifier is shown in Fig. 1. The active device is the MRF183 LDMOS from Freescale Semiconductor Inc., Austin, TX. The series *LC* tank resonates at the input-drive frequency f_{in}, which must be the same as the oscillation frequency, i.e., $f_o = 410$ MHz. Note that the detuning inductance L_{detune} required for the zero voltage switching (ZVS) [15] is separated from the *LC* tank. The input-drive level (V_{in}) and the output circuit parameters ($C_{\mathrm{out}}, Q_{\mathrm{res}}, L_{\mathrm{detune}}$, and R_{L}) are optimized so that the amplifier achieves a proper class-E tuning, which leads to high drain efficiency.

The loaded Q factor of the series resonator Q_{res} is set to 18. This is higher than usual in class-E amplifiers, where the Q is usually below 10. The higher Q increases losses slightly, but helps to obtain a more stable oscillation. C_{out} and L_{detune} can be calculated using the well-known class-E design equations [15]

$$C_{\mathrm{out}} = \frac{0.1836}{2\pi f_{\mathrm{in}} R_L} \tag{1}$$

$$L_{\mathrm{detune}} = \frac{1.1525 R_L}{2\pi f_{\mathrm{in}}}. \tag{2}$$

Assuming 2 Ω for R_L, the equations give $C_{\mathrm{out}} = 36$ pF and $L_{\mathrm{detune}} = 0.9$ nH. Since this transistor already has an output capacitance that is near 36 pF [16], C_{out} is completely absorbed into the transistor.

Starting from these initial values, an HB optimization is performed next using the nonlinear transistor model provided by the vendor. The considered value of the input-drive amplitude is $V_{\mathrm{in}} = 40$ V for which the transistor operates in the saturated region. For the HB simulation, 11 harmonic components are taken into account. Contour plots of constant output power and constant drain efficiency are traced, respectively, as functions of L_{detune} and R_L, shown in Fig. 2. As can be seen, the optimum element values to achieve the highest drain efficiency are not the same as the ones providing the highest output power. The output power keeps increasing until L_{detune} becomes zero, whereas a small detuning inductance is required to satisfy the ZVS condition for the highest drain efficiency. This is due to the fact that the output power has its maximum value at the net resonance frequency of the output *LC* tank including L_{detune}. We choose $L_{\mathrm{detune}} = 0.6$ nH and $R_L = 2.6\ \Omega$, which give the highest efficiency at the expense of some loss of output power.

After setting L_{detune} and R_L to the above optimum values obtained for $V_{\mathrm{in}} = 40$ V, the influence of the input-drive level is analyzed. A sweep in V_{in} is carried out, the results of which are shown in Fig. 3. As a compromise between the saturated operation and the maximum voltage rating of the transistor, the initially considered value $V_{\mathrm{in}} = 40$ V is chosen. This provides an output power of 58 W and a drain efficiency of 73%.

B. Synthesis of Embedding Network

Once the HB optimization of the amplifier has been carried out, the next step is to synthesize the embedding network from the terminal voltages and currents at the reference planes of Fig. 1 (indicated via dashed lines). For convenience, both the transmission line $\mathrm{TL}_{\mathrm{in}}$ and the series *LC* tank are taken inside the reference planes. This choice of the output-reference plane facilitates the synthesis of the embedding network. Although the optimum terminal voltages and currents are calculated with 11 harmonic components, the strong bandpass-filtering action of the *LC* tank allows a synthesis of the embedding network at the fundamental frequency only, without substantial degradation of the design accuracy. At all other harmonic frequencies, the drain of the transistor will be terminated by a shunt capacitance or C_{out}, which is the proper harmonic loading for a class-E oscillator.

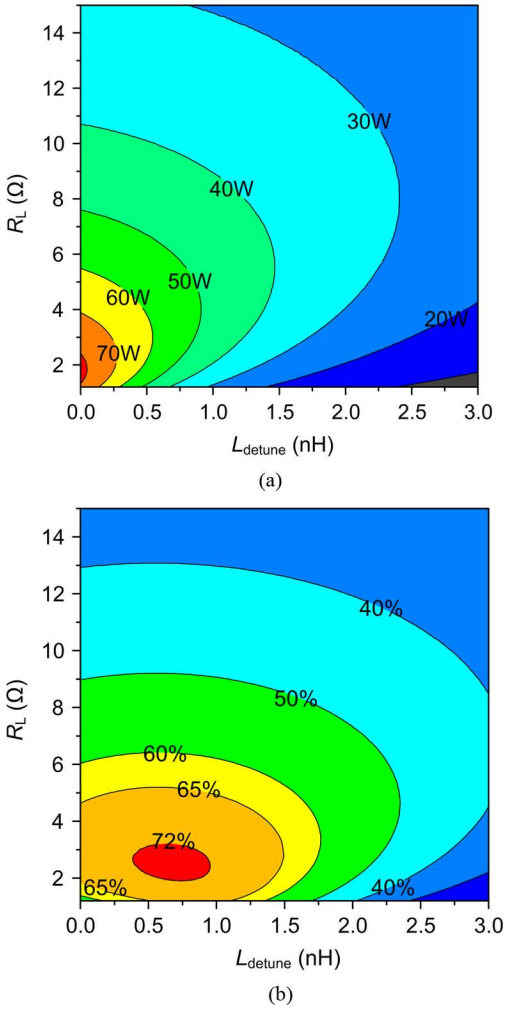

Fig. 2. (a) Simulated output power and (b) drain efficiency of the class-E amplifier as functions of detuning inductance and load resistance. The drain and gate bias voltages are 25 and 4 V, respectively.

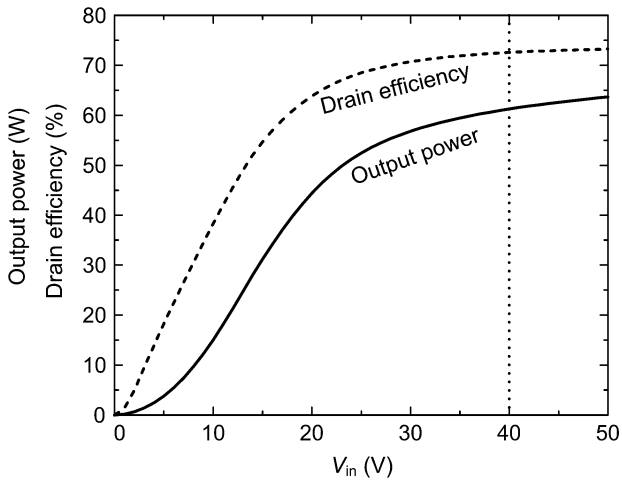

Fig. 3. Simulated output power and drain efficiency as a function of the input-drive level $V_{\rm in}$. $L_{\rm detune}$ and R_L are tuned to the maximum drain efficiency point. The dotted line at 40 V represents the determined input-drive level for the saturated operation.

The embedding network is usually configured as a T-network or Π-network [11]. In this study, a Π-network is chosen,

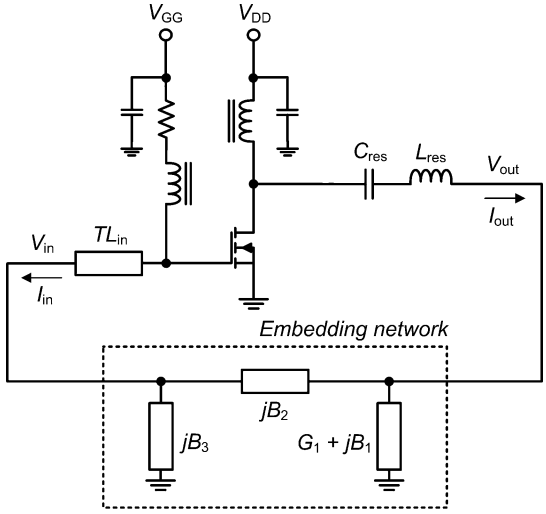

Fig. 4. Basic structure of the class-E oscillator consisting of a transistor, a series *LC* tank, and an embedding network. The embedding network substitutes for the input-drive source and output load circuitry of the class-E amplifier in Fig. 1, keeping the same set of terminal voltages and currents.

as shown in Fig. 4. It consists of three reactive elements (jB_1, jB_2, jB_3) and one resistive element (G_1) representing the load resistance. For this particular network, the two-port Y-parameters relating the terminal currents $I_{\rm in}, I_{\rm out}$ and voltages $V_{\rm in}, V_{\rm out}$ are

$$\begin{bmatrix} I_{\rm in} \\ I_{\rm out} \end{bmatrix} = \begin{bmatrix} j(B_2+B_3) & -jB_2 \\ -jB_2 & G_1 + j(B_1+B_2) \end{bmatrix} \begin{bmatrix} V_{\rm in} \\ V_{\rm out} \end{bmatrix}. \tag{3}$$

Thus, the four element values are calculated in terms of the terminal voltages and currents as follows:

$$\begin{bmatrix} B_2 \\ B_3 \end{bmatrix} = \begin{bmatrix} {\rm Im}\{V_{\rm out}\} - {\rm Im}\{V_{\rm in}\} & -{\rm Im}\{V_{\rm in}\} \\ {\rm Re}\{V_{\rm in}\} - {\rm Re}\{V_{\rm out}\} & {\rm Re}\{V_{\rm in}\} \end{bmatrix}^{-1} \begin{bmatrix} {\rm Re}\{I_{\rm in}\} \\ {\rm Im}\{I_{\rm in}\} \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} G_1 \\ B_1 \end{bmatrix} = \begin{bmatrix} {\rm Re}\{V_{\rm out}\} & -{\rm Im}\{V_{\rm out}\} \\ {\rm Im}\{V_{\rm out}\} & {\rm Re}\{V_{\rm out}\} \end{bmatrix}^{-1} \times \begin{bmatrix} {\rm Re}\{I_{\rm in}+I_{\rm out}\} + B_3{\rm Im}\{V_{\rm in}\} \\ {\rm Im}\{I_{\rm in}+I_{\rm out}\} - B_3{\rm Re}\{V_{\rm in}\} \end{bmatrix}. \tag{5}$$

In order for (4) and (5) to be solvable, the matrices on the right-hand side must be invertible (not singular). As derived in [11], this requires two conditions, easily fulfilled by the amplifier: $V_{\rm out}$ must not be zero and a phase difference between $V_{\rm in}$ and $V_{\rm out}$ must exist. The element values for the T-network could also be derived in a similar way.

The fundamental components of the terminal voltages and currents of the optimized amplifier in Section II-A are shown in Table I. The phase of $V_{\rm in}$ is set to 0° without loss of generality. The element values of the embedding network, obtained from (4) and (5), are shown in Table II. As can be seen, the network will be composed of two capacitors for B_2 and B_3, an inductor

TABLE I
OPTIMIZED TERMINAL VOLTAGES AND CURRENTS AT FUNDAMENTAL FREQUENCY

V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)
$40.0e^{j0°}$	$2.6e^{j91.3°}$	$19.9e^{-j5.8°}$	$6.9e^{-j52.1°}$

TABLE II
EVALUATED ELEMENT VALUES OF EMBEDDING NETWORK AND CORRESPONDING CIRCUIT ELEMENTS

Element	G_1	B_1	B_2	B_3
Evaluated value	302.9 mS	-147.5 mS	6.7 mS	60.6 mS
Circuit element	$R_1 = 3.3\ \Omega$	$L_1 = 2.6$ nH	$C_2 = 2.6$ pF	$C_3 = 23.5$ pF

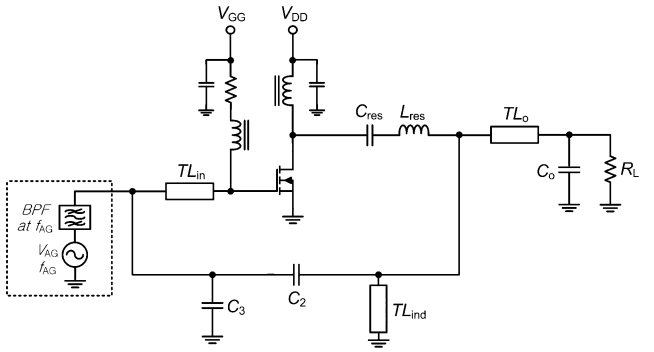

Fig. 5. Complete schematic of the class-E oscillator. The embedding network is implemented by capacitors (C_2, C_3, C_o), transmission lines $(\text{TL}_{\text{ind}}, \text{TL}_o)$, and a 50-$\omega$ load (R_L). The AG, consisting of a voltage source and an ideal bandpass filter inside the dashed box, is not a part of the oscillator, but will be used for the nonlinear simulation of oscillatory solutions in Section III.

for B_1, and a resistive component transformed from the output load.

Fig. 5 shows the complete schematic of the class-E oscillator with the implemented embedding network. A shunt transmission line of 110-Ω characteristic impedance (TL_{ind}) is used for the implementation of L_1. The 50-Ω output load is transformed to R_1 by a simple L-section matching ($C_o = 28$ pF and a transmission line TL_o) [17]. This oscillator configuration with the determined element values will serve as the starting point for the new nonlinear optimization, which will be presented in Section III.

III. NONLINEAR OPTIMIZATION OF THE OSCILLATOR PERFORMANCE

In Section II, the class-E oscillator was optimized in terms of the output power and efficiency, taking into account the saturated operation of the transistor. However, the design has two intrinsic limitations. As already stated, the synthesis of the embedding network is carried out, considering only the fundamental frequency. In spite of the judicious choice of the output-reference plane to reduce the influence of the other harmonic components, the approach is not appropriate to accurately predict the performance of switching-mode oscillators in which many harmonics are strongly generated. Moreover, the onset of the oscillation from a small-signal level is not guaranteed by the steady-state oscillation condition. The oscillation startup should be investigated separately to check whether or not the oscillation is truly triggered and growing to the designed power level.

To overcome those limitations, a new optimization technique taking into account all the generated harmonic components will be employed, together with the stability analysis based on pole-zero identification [13].

A. Nonlinear Optimization Through the AG Technique

The AG technique was initially proposed to avoid trivial solutions in the HB simulation of autonomous circuits [12]. However, the AG can also be used for nonlinear oscillator design at a specific frequency using HB. The AG, composed of a voltage source and a bandpass filter in series (Fig. 5), is connected in parallel at a circuit node. The AG frequency is made equal to the oscillation frequency $f_{\text{AG}} = f_o$. The series bandpass filter is an ideal short circuit at f_{AG} and an open circuit at all the other frequencies. Thus, the AG amplitude V_{AG} agrees with the fundamental component of the voltage amplitude at the connection node. Since the AG is introduced only for simulation purposes, it should have no influence on the steady-state oscillatory solution. This is imposed by the following nonperturbation condition:

$$Y_{\text{AG}} = I_{\text{AG}}/V_{\text{AG}} = 0 \tag{6}$$

where I_{AG} is the current through the AG at f_{AG}. Equation (6) is solved through error-minimization or optimization procedures with the HB system as the inner loop.

For the optimization of the power oscillator, the AG is connected to the same node considered in the definition of the input-reference plane in Fig. 1. Thus, the AG amplitude V_{AG} is made equal to the input-drive amplitude $V_{\text{in}} = 40$ V obtained in Section II, i.e., $V_{\text{AG}} = 40$ V. In this way, the transistor is in deep saturation during the nonlinear simulation, which leads to the switching-mode operation of the oscillator. The AG frequency f_{AG} is set to the desired oscillation value of 410 MHz. With both the AG amplitude and frequency imposed by the designer, two circuit element values must be determined in order to fulfill the nonperturbation condition (6). In our oscillator, two capacitors in the feedback network, i.e., C_2 and C_3, are calculated. The rest of elements are set to the values obtained in Table II. Equation (6) is solved through optimization in HB, considering 11 harmonic components. The simulation predicts 61-W output power with 71% dc-to-RF conversion efficiency for the imposed V_{AG} value, $V_{\text{AG}} = 40$ V. This agrees well with the amplifier performance for the same input-drive voltage $V_{\text{in}} = 40$ V in Section II-A.

To investigate the influence of the feedback-element values on the oscillator performance, two nested sweeps are carried out in C_2 and C_3. For each pair of capacitance values (C_2, C_3), the oscillation amplitude V_{AG} and the capacitance (or the inductance) in the series *LC* tank, i.e., C_{res} (or L_{res}) are optimized in order to fulfill the nonperturbation condition $Y_{\text{AG}} = 0$. It is important to note that the oscillation frequency keeps the desired value during the entire double sweep, which is ensured by setting the AG frequency to $f_{\text{AG}} = 410$ MHz. In contrast, the oscillation amplitude is modified during the sweep since V_{AG} is

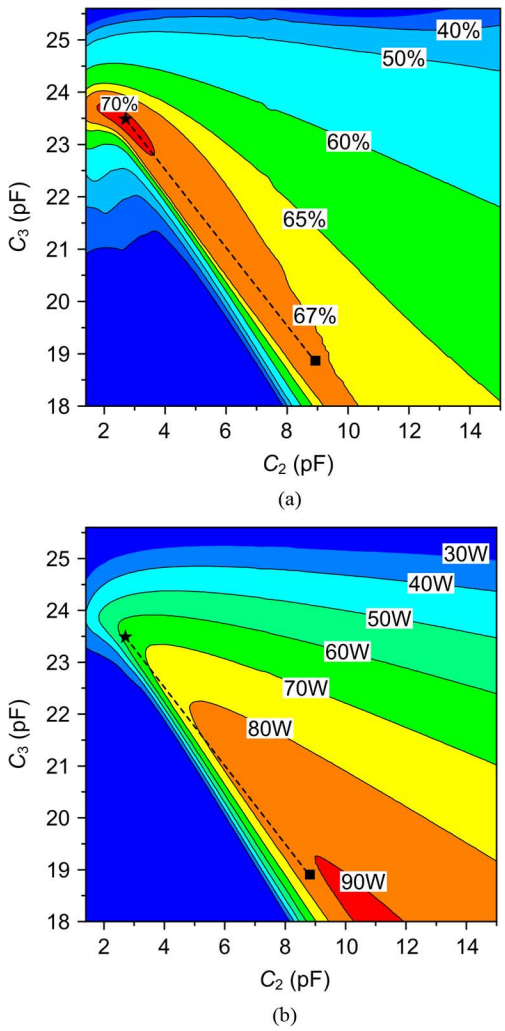

Fig. 6. Contour plots of the: (a) simulated dc-to-RF conversion efficiency and (b) output power in the plane of (C_2, C_3). For the entire solutions, the oscillation frequency is fixed to 410 MHz. The points of a star and a square represent, respectively, the original values of (C_2, C_3) obtained in Section II and the new values nonlinearly optimized in the output power and efficiency.

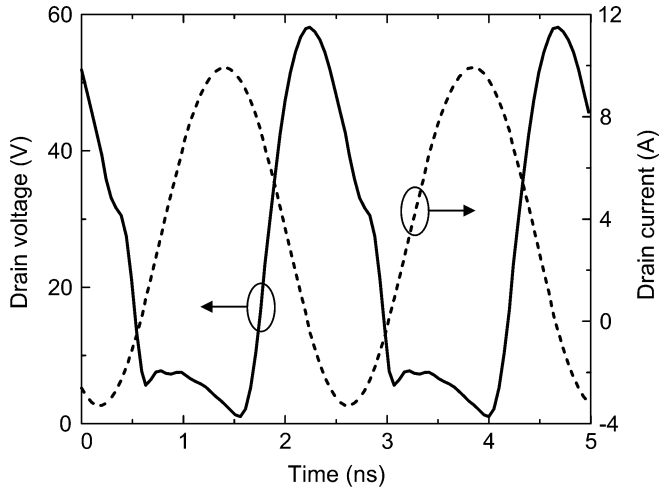

Fig. 7. Simulated voltage and current waveforms at the extrinsic drain terminal, corresponding to the square point in Fig. 6. The drain and gate bias voltages are 25 and 4 V, respectively.

one of the considered optimization variables, together with $C_{\rm res}$ (or $L_{\rm res}$).

The simulated contours of constant output power and constant efficiency in the plane of (C_2, C_3) are shown in Fig. 6. The efficiency in Fig. 6(a) exhibits its maximum value near the point resulting from the quasi-nonlinear analysis, corresponding to 2.6 pF of C_2 and 23.5 pF of C_3 (marked by a star). It means that the effect of harmonic components on the efficiency is not too significant in this class-E oscillator. This is mainly due to the series *LC* tank with a high-Q factor, which prevents the harmonics generated at the drain from affecting the output load. This confirms the assumptions in the synthesis technique discussed in Section II-B. It is also interesting to see that the contour plot in Fig. 6(a) has a narrow ridge of the efficiency along the dashed line. By changing (C_2, C_3) along this line, the oscillator output power could be optimized further, maintaining a high efficiency of more than 67%.

As can be seen in Fig. 6(b), the output power does not show its peak at the point marked with a star, but keeps increasing along the dashed line toward the point marked with a square. Hence, the feedback elements can be modified from the original values determined in Section II in order to obtain a higher output power without impairing the efficiency significantly.

For the circuit-element values corresponding to the square point ($C_2 = 9.0$ pF, $C_3 = 18.7$ pF), the oscillation amplitude fulfilling the nonperturbation condition (6) at the imposed frequency $f_{\rm AG0} = 410$ MHz is $V_{\rm AG0} = 97$ V. The predicted output power is 85 W with 68% dc-to-RF conversion efficiency. We did not want to further increase the output power because the transistor might become too hot. Fig. 7 shows the simulated voltage and current waveforms at the extrinsic drain terminal. Due to the series *LC* tank and the complete absorption of $C_{\rm out}$ into the transistor output capacitance, the drain current exhibits an almost sinusoidal waveform.

The above analysis and optimization are applied to the circuit in its steady-state oscillatory regime. However, even if the obtained solutions are accurate and valid, the oscillator might fail to start up from its dc solution with the optimized values of the circuit elements. The oscillation startup from the dc regime is due to the instability of the dc solution at the oscillation frequency. Thus, the startup condition depends on this dc solution and its stability properties. The stability of the dc solution and that of the steady-state oscillatory solution must be separately analyzed, as will be shown in Section III-B.

B. *Stability Analysis*

To verify the oscillation startup, the stability of the dc solution, coexisting with this oscillation, must be analyzed. This is done with the pole-zero identification technique [13], which, in the case of a dc solution, requires the calculation of the input impedance function $Z_{\rm in}(f)$ at a given circuit node through ac analysis. A sweep in the frequency f is carried out, applying pole-zero identification to the resulting function $Z_{\rm in}(f)$. In our class-E oscillator, the considered observation port, at which $Z_{\rm in}(f)$ is calculated, is defined between the gate node and ground.

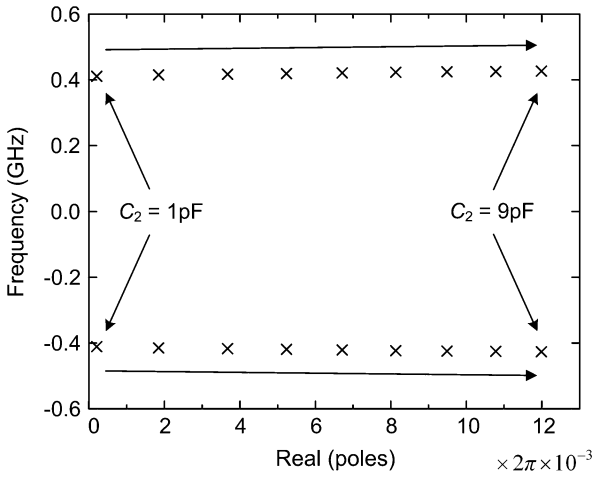

Fig. 8. Evolution of the critical pole pair with the values of C_2 and C_3 varied along the dashed line in Fig. 6. C_2 is varied from 1 to 9 pF in steps of 1 pF along the dashed line and the corresponding value of C_3 is calculated from the dashed-line equation.

For the stability analysis, the parameters C_2 and C_3 are varied along the dashed line in Fig. 6 by changing C_2 in 1-pF steps and calculating the corresponding C_3 from the linear equation of the dashed line. Pole-zero identification is applied to the dc solution associated with each pair of values C_2 and C_3. For all the points in the line, a pair of complex-conjugate poles, with frequency close to the oscillation frequency, is located on the right-hand side of the complex plane. The evolution of this critical pair of poles along the dashed line is shown in Fig. 8. All the pairs are located on the right-hand side of the plane with a nearly constant imaginary part. This implies that all the points along the dashed line satisfy the oscillation startup condition around 410 MHz. The nearly constant value of this frequency is explained by the fact that the oscillation frequency was kept constant at the nonlinear design stage by setting $f_{\rm AG} = 410$ MHz. However, the real part of the pole pair, indicating the instability margin for startup, is very small at low values of C_2 and increases as (C_2, C_3) approaches the square point along the line. This means that the square point is less likely to be affected in startup by inaccuracies of the circuit model.

The stability of the steady-state oscillation at this optimum point must also be analyzed, which will also be carried out using the pole-zero identification technique [13]. For this analysis, the AG is maintained at the amplitude $V_{\rm AG}^0 = 97$ V and frequency $f_{\rm AG}^0 = 410$ MHz, which fulfill $Y_{\rm AG} = 0$ at the point marked with a square in Fig. 6. A small-signal current source at frequency f is then added to the circuit. By the conversion-matrix approach, the impedance function $Z_{\rm in}(f)$ is calculated as the ratio between the node voltage and the introduced current [13]. Pole-zero identification is applied to this impedance function. For a rigorous analysis, several frequency intervals are considered in the range from 0 to $f_{\rm AG}^0$. When sweeping near $f_{\rm AG}^0$, a pair of complex-conjugate poles at this oscillation frequency is located on the imaginary axis, as expected in an oscillatory regime [12]. The rest of poles, for all the different frequency sweeps, are located on the left-hand side of the complex plane, which indicates a stable oscillation.

IV. Analysis of the Oscillating Solution Versus the Gate Bias

Typically, class-E amplifiers and oscillators exhibit higher efficiency for gate bias below the threshold voltage. However, in the case of oscillators, the startup does not occur for gate bias below this threshold because no actual gain is exhibited by the transistor and, thus, the dc solution is stable. Nevertheless, after the oscillation buildup for gate bias above the threshold voltage, it might be possible to experimentally reduce this bias voltage below the threshold while the oscillatory regime is still observed. This may lead to an oscillation with higher efficiency. As an example, a triggering signal is used in [18] to start up a high-efficiency oscillation at low gate bias voltage. The requirement for this signal must be due to the coexistence of the desired oscillatory regime with a stable dc solution.

The evolution of the steady-state oscillation when reducing the gate bias is analyzed here using an AG. For the simulation, the element values of the optimized design corresponding to the square point in Fig. 6 are considered. The gate bias is reduced from $V_{gg} = 5$ V, calculating, at each sweep step, the oscillation amplitude $V_{\rm AG}$ and frequency $f_{\rm AG}$ in order to fulfill the nonperturbation condition $Y_{\rm AG}(V_{\rm AG}, f_{\rm AG}) = 0$. When performing this gate-bias sweep, the bias can be reduced below the threshold voltage with the HB solution still converging to a steady-sate oscillation. A switching-parameter algorithm [12] must be applied to obtain the entire oscillation curve. Below a certain gate bias, the AG amplitude is swept instead of V_{gg} and reduced to zero, determining, at each sweep step, the bias voltage V_{gg} and oscillation frequency $f_{\rm AG}$ in order to fulfill the nonperturbation condition $Y_{\rm AG}(V_{gg}, f_{\rm AG}) = 0$.

In Fig. 9, the oscillation curve has been traced for four different values of the drain bias voltage. Fig. 9(a) shows the output power variation and Fig. 9(b) shows the efficiency variation versus the gate bias. Each curve has a turning point that divides it into a stable and an unstable section. As will be shown later, the solid-line section corresponds to stable solutions, whereas the dashed-line section corresponds to unstable ones. All curves start from zero amplitude at the threshold voltage $V_{gg} = 3.2$ V. At this voltage value, a Hopf bifurcation takes place in the dc solution [12], i.e., a pair of complex-conjugate poles at the oscillation frequency crosses the imaginary axis. The dc solution is unstable above the threshold voltage. The Hopf bifurcation is of subcritical type [12], [19]. Thus, after the bifurcation, no stable oscillation exists in the neighborhood of the dc solution, which gives rise to a jump to the upper section of the oscillation curve in Fig. 9. On the other hand, when the gate bias is reduced from a voltage above the threshold, the oscillation persists until it reaches the turning point, below which no oscillation is possible. Thus, a hysteresis phenomenon is obtained versus the gate bias.

The stability of the oscillation curves in Fig. 9 has been analyzed with pole-zero identification. A turning point in a periodic-solution curve corresponds to the Floquet multiplier crossing the unit circle through $1 + j0$ [19]. Due to the nonunivocal relationship between poles and multipliers, this is equivalent to the simultaneous crossing of the imaginary axis by a real pole and infinite pairs of poles $\pm jkf_o$ with k being a positive integer and f_o being the oscillation frequency [19]. For the pole-zero identification, a frequency sweep about f_o

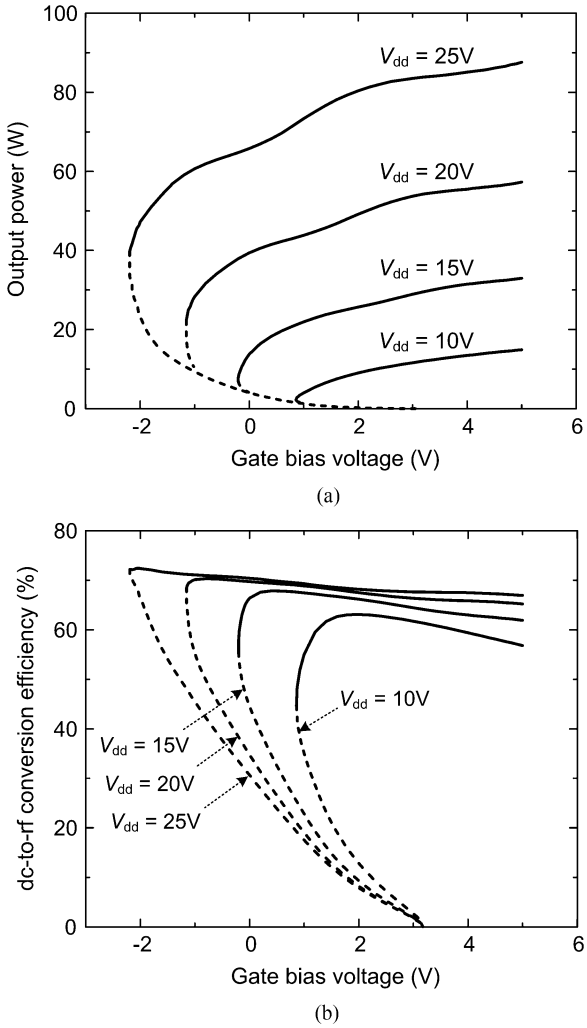

Fig. 9. Simulated output power and dc-to-RF conversion efficiency in the oscillatory regime as a function of the gate bias voltage. Four drain bias voltages (V_{dd}) are considered. The solid- and dashed-line sections represent the stable and unstable oscillating solutions, respectively, in each solution curve.

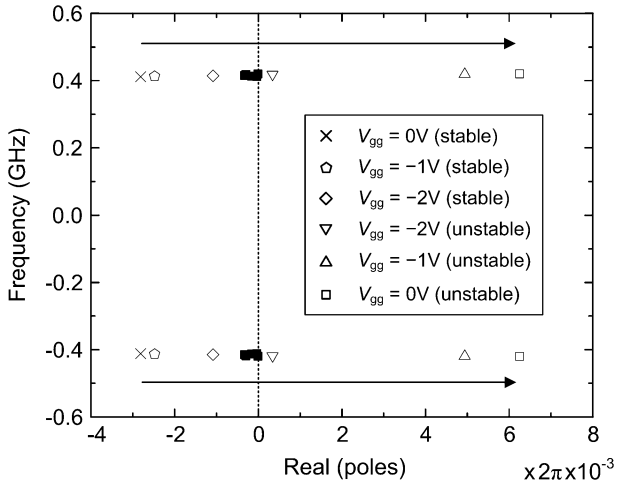

Fig. 10. Evolution of the critical pole pair for the steady-state oscillating solution as the gate bias varies from the stable section to the unstable one near the turning point in Fig. 9. The solid squares close to the imaginary axis represent another pair of complex-conjugate poles at each bias point, exhibited due to the singularity of the HB system for oscillating solutions.

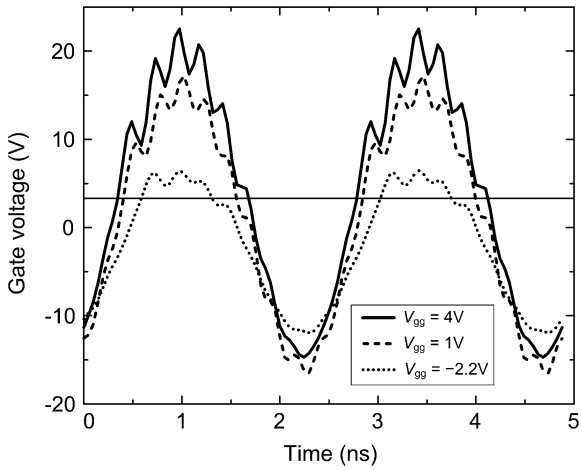

Fig. 11. Gate voltage waveforms at different gate bias voltages. The threshold voltage is represented by a thin solid line. The considered drain bias is 25 V.

will be initially considered. Near the turning point, a pair of complex-conjugate poles $\sigma \pm jf_o$ is obtained at the oscillation frequency. This is an additional pair of poles different from the one located on the imaginary axis at $\pm jf_o$, which exists for all points in the curve due to the solution autonomy.

In the solid-line section of Fig. 9, near the turning point, the pair of poles $\sigma \pm jf_o$ is located on the left-hand side of the complex plane. When varying the gate bias from the solid-line section to the dashed-line one around the turning point, the pair of poles approaches the imaginary axis and crosses it at the turning point. The pair of poles $\sigma \pm jf_o$ then stays on the right-hand side for all the entire dashed-line section, thus this section is unstable. This is shown in the pole locus of Fig. 10, corresponding to $V_{dd} = 25$ V. For all the considered solution points, another pair of poles at f_o, very close to the imaginary axis, is also obtained. This is represented by solid squares. It must be pointed out that to clearly obtain the two distinct pairs of poles at $\pm jf_o$ and $\sigma \pm jf_o$, high accuracy is necessary in the HB calculation of the steady-state oscillating solution.

The hysteresis in the oscillation curves of Fig. 9 comes from the fact that a high power oscillation is built up when the gate bias reaches the threshold voltage. This is related with the high input-drive voltage considered in the initial amplifier design of Section II in order to ensure the switching-mode operation. In the oscillator design, the embedding network is synthesized from the terminal voltages and currents associated with this high-amplitude solution. Once the oscillation builds up at gate bias above the threshold, there exists a high-amplitude oscillating signal at the gate over the quiescent gate bias voltage. This signal turns the transistor on and off as in a switch, as shown in Fig. 11 (the solid waveform). When the gate bias is reduced below the threshold voltage, this self-generated input-drive signal decreases in a continuous manner so it is still large enough to make the transistor operate as a switch (see the dashed waveform in Fig. 11). The situation is different when the gate bias is increased from a dc regime. In that case, no oscillation is possible until the threshold is reached because there is no input-drive signal to the transistor.

When the gate bias is decreased to the turning point, the self-generated input-drive signal becomes marginal to turn on the transistor and thus to sustain the steady-state oscillation (see

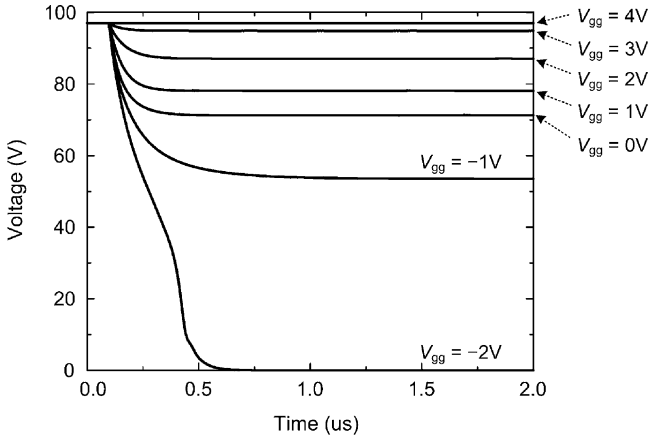

Fig. 12. Simulated evolution of the oscillating solution as the gate bias changes from 4 V to different values. The fundamental component of the voltage at the AG connection node is represented. The AG is disconnected at 0.1 μs. The considered drain bias is 25 V.

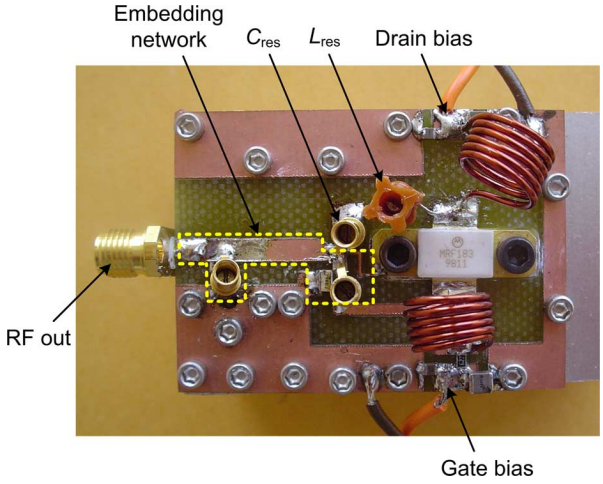

Fig. 13. Class-E oscillator built on FR-4 board. The transistor is mounted directly on a heatsink through a slot in the board. The circuit size is 49 mm × 35 mm.

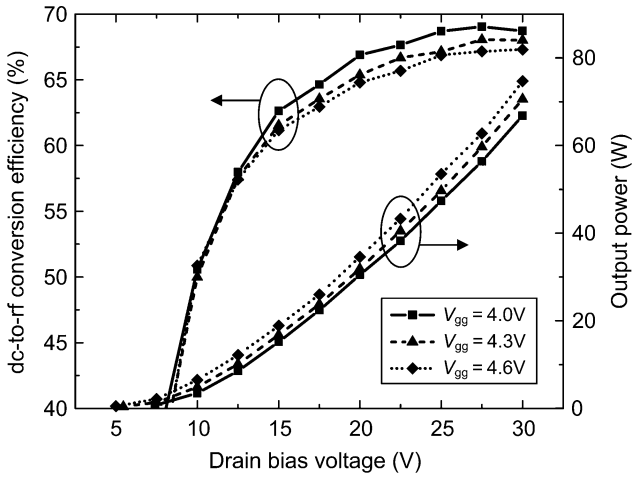

Fig. 14. Measured output power and dc-to-RF conversion efficiency versus the drain bias voltage.

the dotted waveform in Fig. 11). If the gate bias is further decreased, no oscillation is observed. As can be seen in Fig. 9, and in agreement with the previous discussion, the gate bias voltage at the turning point decreases with the drain bias because a larger swing is obtained in the gate voltage waveform.

In switching-mode amplifiers and oscillators, the output power is usually modified by varying the drain-bias voltage [5], [7], [9], [20], [21]. The reduction of output power, which might be required for some applications, is achieved by decreasing the drain bias, which generally gives rise to a severe degradation of the drain efficiency [5], [7], [9], [21]. This can be avoided by taking advantage of the possibility to maintain the oscillation at the gate bias below the threshold voltage. It enables the reduction of the output power without the efficiency degradation. As shown in Fig. 9(a), the output power decreases as the gate bias approaches the turning point. The efficiency, however, increases with lower gate bias [see Fig. 9(b)], as expected in a class-E oscillator. Hence, the output power can be varied by changing the gate bias down to the turning point, which provides higher efficiency. It must be noted, however, that the stable oscillation and the stable dc solution coexist in the interval comprised between the turning point and the Hopf bifurcation. Each of these two stable solutions has its own basin of attraction in the phase space [12]. Thus, the oscillatory solution will be robust under noise and small perturbations, but a big perturbation such as a high amplitude pulse may lead the system back to the stable dc solution.

For a rough test for the robustness of the oscillation below the threshold voltage, envelope-transient simulations [22], [23] are performed. A sweep is carried out in the gate bias, which is reduced from $V_{gg} = 4$ V to lower values. At each bias-sweep step, the HB solution corresponding to $V_{gg} = 4$ V is used as the initial value for the envelope-transient equations. Actually, an AG with the steady-state values $V_{\rm AG}^0 = 97$ V and $f_{\rm AG}^0 = 410$ MHz, corresponding to $V_{gg} = 4$ V, is connected to the circuit for a short initial time interval and disconnected afterwards. This disconnection is carried out with a time-varying resistor [24]. Fig. 12 shows the time variation of the first harmonic amplitude of the voltage at the AG connection node. At 0.1 μs, the AG is disconnected for all the V_{gg} values. After a certain transient time, each solution reaches the steady-state amplitude, which decreases with smaller V_{gg}, as expected from Fig. 9. When V_{gg} is reduced below the turning point, e.g., −2 V, the oscillation is extinguished.

The simulation of Fig. 12 shows that, below the threshold voltage, stable oscillation can be reached even when the initial conditions are not in the immediate neighborhood of the steady-state values. The robustness of the oscillation will actually depend on the size of the basin of attraction for this solution in the phase space [12], which would be extremely difficult to determine.

V. Experimental Results

The class-E oscillator designed following the proposed technique is fabricated on FR-4 board. Fig. 13 presents a photograph of the oscillator mounted on a heatsink. An air-core inductor from Coilcraft, Cary, IL, with a current rating of 7.2 A is used for the inductor in the output *LC* tank. For tuning purposes, Giga-Trim variable capacitors from Johanson, Boonton, NJ, are

TABLE III
PERFORMANCE COMPARISON OF PUBLISHED SWITCHING-MODE OSCILLATORS

Oscillation frequency	Output power	Efficiency	Class	Reference
2 MHz	3 W	95 %	E	[3]
800 kHz	1.19 W	86 %	E	[4]
5 GHz	0.47 W	56 %	E	[5]
1.6 GHz	0.25 W	67 %	F	[6]
915 MHz	65 W	65 %	Not specified	[7]
1.86 GHz	< 0.03 W	61 %	Between B and F	[8]
6 GHz	Not specified	48 %	F	[9]
410 MHz	**75 W**	**67 %**	**E**	**This work**
410 MHz	**67 W**	**69 %**	**E**	**This work**

employed along with ATC multilayer capacitors. Initially, the capacitors are tuned to the values synthesized in Section II-B (marked by the star in Fig. 6). No oscillation starts up with these component values, which is partly attributed to a small instability margin predicted in Fig. 8.

The capacitors are then tuned to the nonlinearly optimized values obtained in Section III (marked by the square in Fig. 6), which are 9.0 pF for C_2 and 18.7 pF for C_3. The output power is measured by a Bird 4022 power sensor and a 4421 power meter. Fig. 14 shows the measured output power and dc-to-RF conversion efficiency versus the drain bias voltage at three different gate bias voltages. The gate biases are slightly above the threshold voltage of the transistor to give a free-running oscillation. The output power increases as the square of the drain bias, as expected in a switching-mode operation [20]. The efficiency increases rapidly at low drain bias and saturates at high drain bias. As the gate bias increases, the efficiency is reduced, but the oscillator exhibits higher output power. This is due to the fact that the class-E tuning shows the highest efficiency with the gate bias below the threshold voltage. The oscillator achieves the highest efficiency of 69% with 67-W output power, and 67% efficiency with 75 W at higher bias voltage. These results are compared with those of other switching-mode oscillators of high efficiency in Table III.

The hysteresis in terms of the gate bias is also experimentally verified. After the oscillation builds up at a gate bias of 4 V, the bias voltage is reduced gradually down to 0 V. The oscillation is sustained for all the gate bias voltages. Fig. 15 shows the measured output power and efficiency versus the gate bias. The output power decreases when the gate bias is reduced, whereas the efficiency improves, in comparison with the values corresponding to the gate bias of $V_{gg} = 4$ V.

The output power spectrum, measured by an Agilent E4407B spectrum analyzer, is shown in Fig. 16. The simulated spectrum is superimposed with square marks. The largest harmonic level is 46 dB below the fundamental, which corresponds to the second harmonic component. High-frequency ringing is observed at the fifth and sixth harmonics in the measured spectrum. It is due to a parasitic resonance when the transistor is turned on and off abruptly [25]. The phase noise is −117 dBc/Hz at a frequency offset of 100 kHz.

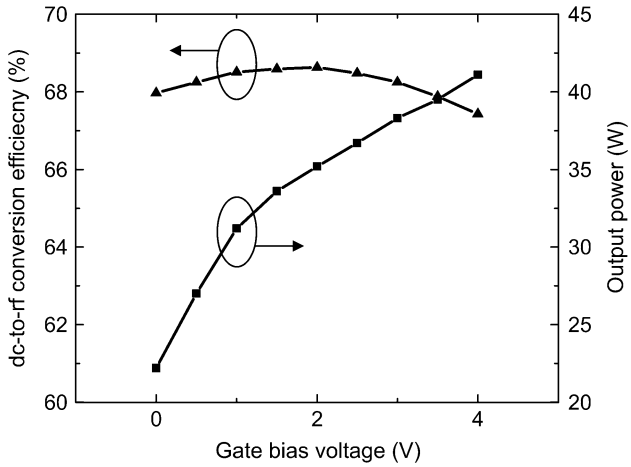

Fig. 15. Measured output power and dc-to-RF conversion efficiency versus the gate bias voltage. The applied drain bias voltage is 23 V.

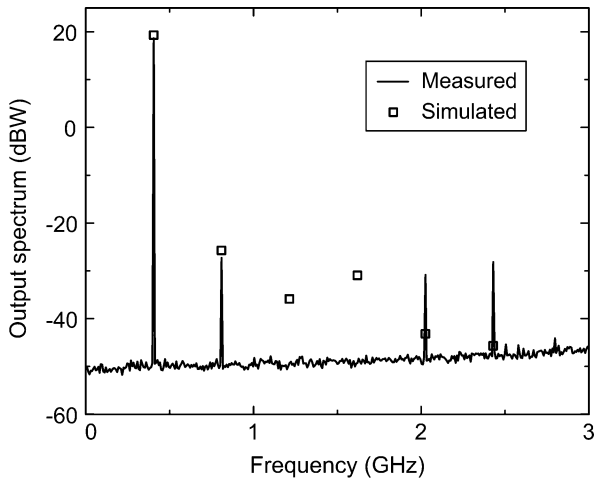

Fig. 16. Measured and simulated output power spectrum. The largest harmonic is the second, which is at 46 dB below the fundamental.

VI. Conclusion

A systematic technique for the nonlinear design of high-power switching-mode oscillators has been presented. The technique is based on the use of an AG on HB. After an initial quasi-nonlinear design, the AG provides the transistor with the required input-drive amplitude for switching operation and allows obtaining the contour plots of constant output power and constant efficiency without affecting the oscillation frequency. Following this technique, a class-E oscillator has been designed and characterized. The oscillation startup and the steady-state stability have been analyzed with pole-zero identification. The influence of the gate bias voltage on the oscillation power and efficiency has been investigated, together with the reasons for the common observation of hysteresis versus the bias. The designed class-E oscillator exhibited 75-W output power with 67% dc-to-RF conversion efficiency.

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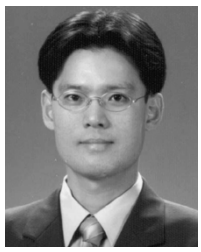

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